Fig.1 (Prior Art)

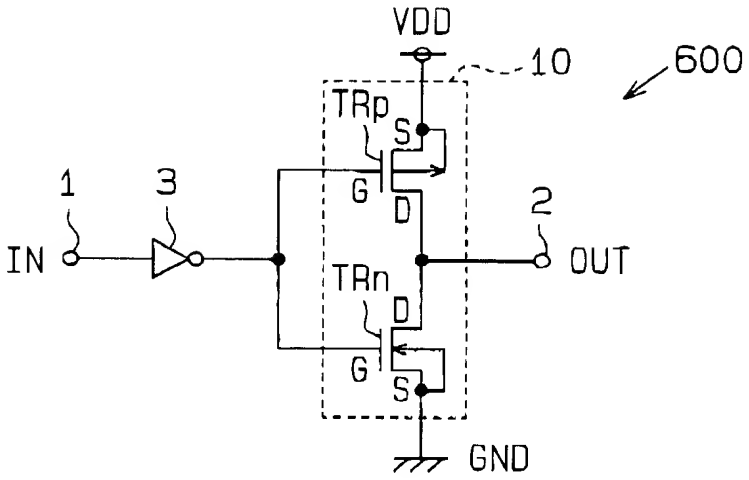


Fig.2

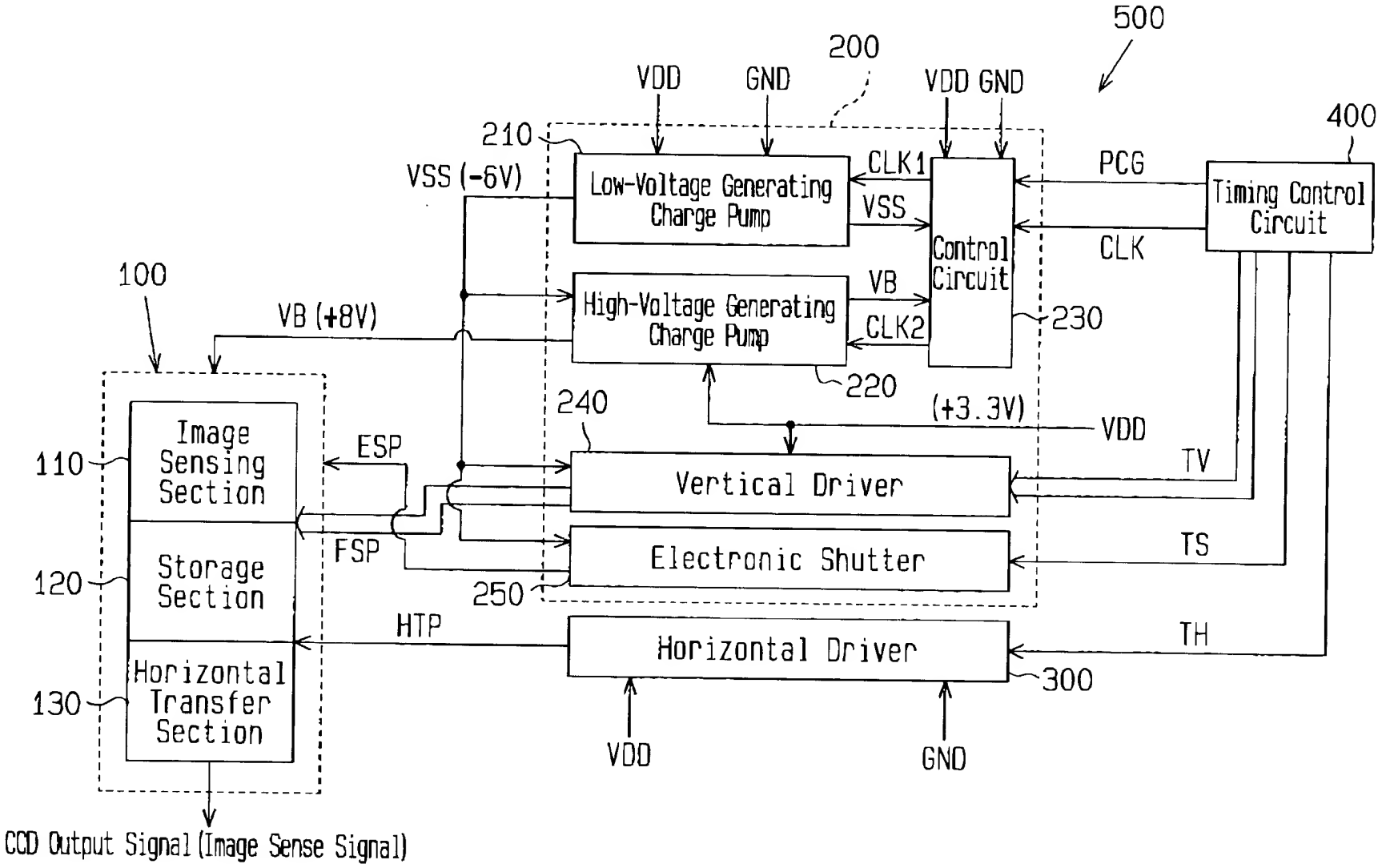
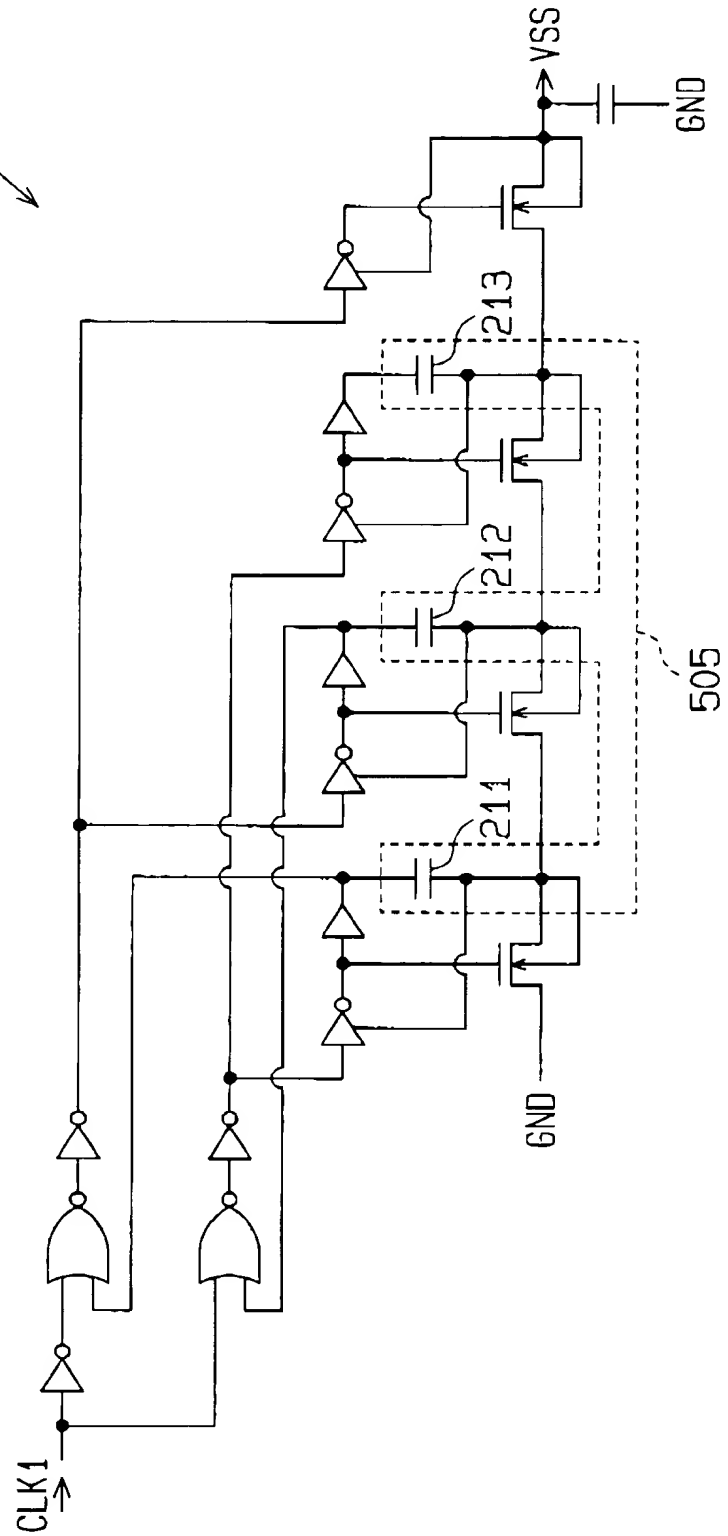

500
200
VDD
GND
VDD GND
400
210
CLK1
PCG
VSS (-6V)
Low-Voltage Generating Charge Pump
VSS
Timing Control Circuit
Control Circuit
CLK
100
VB
VB (+8V)
High-Voltage Generating Charge Pump
CLK2
230
220
240
(+3.3V)
VDD
Image Sensing Section
ESP
110
TV
Vertical Driver
FSP
Storage Section
TS
120
Electronic Shutter
250
HTP
TH
Horizontal Driver
Horizontal Transfer Section
300
130
VDD
GND
CCD Output Signal (Image Sense Signal)

Fig.3



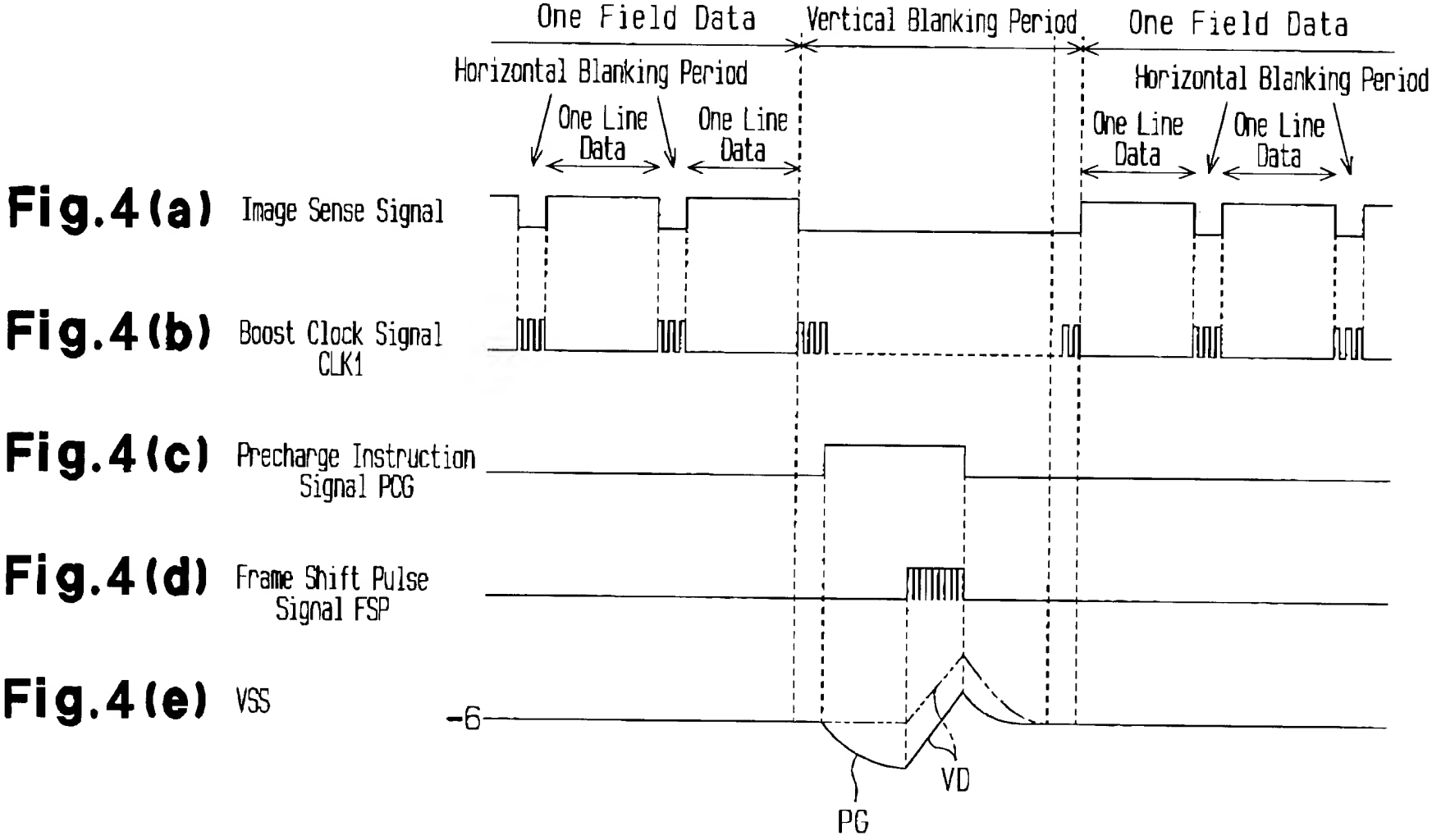

One Field Data
Vertical Blanking Period
One Field Data
Horizontal Blanking Period
Horizontal Blanking Period
One Line Data
One Line Data
One Line Data
One Line Data
Fig.4(a) Image Sense Signal
Fig.4(b) Boost Clock Signal CLK1
Fig.4(c) Precharge Instruction Signal PCG
Fig.4(d) Frame Shift Pulse Signal FSP
Fig.4(e) VSS
-6
VD
PG

Fig.5

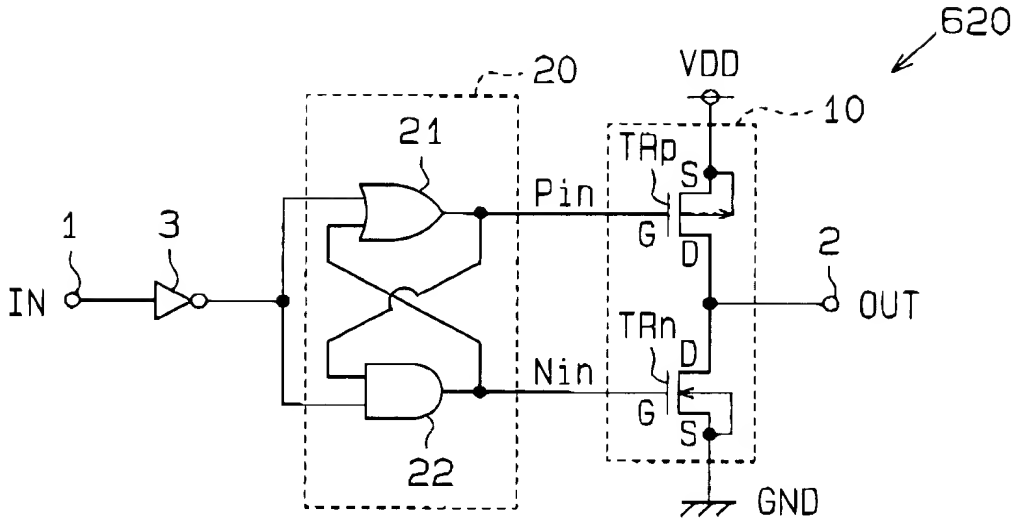


Fig.6(a) IN

Fig.6(b) Pin

Fig.6(c) Nin

Fig.6(d) OUT

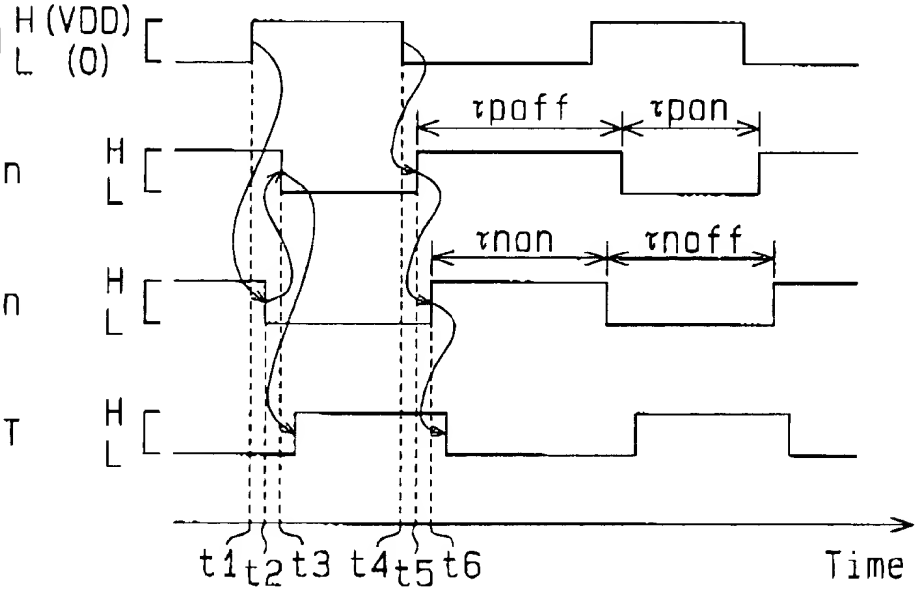


Fig.7

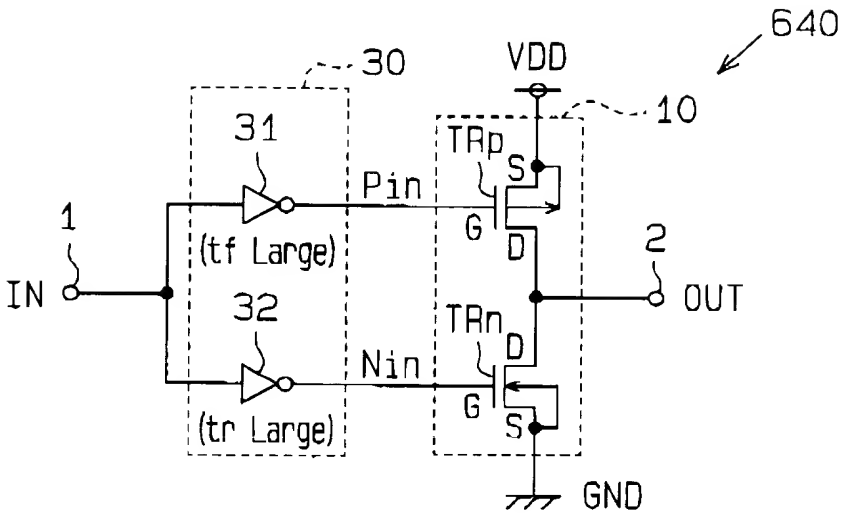


Fig.8(a) IN

Fig.8(b) Pin

Fig.8(c) Nin

Fig.8(d) OUT

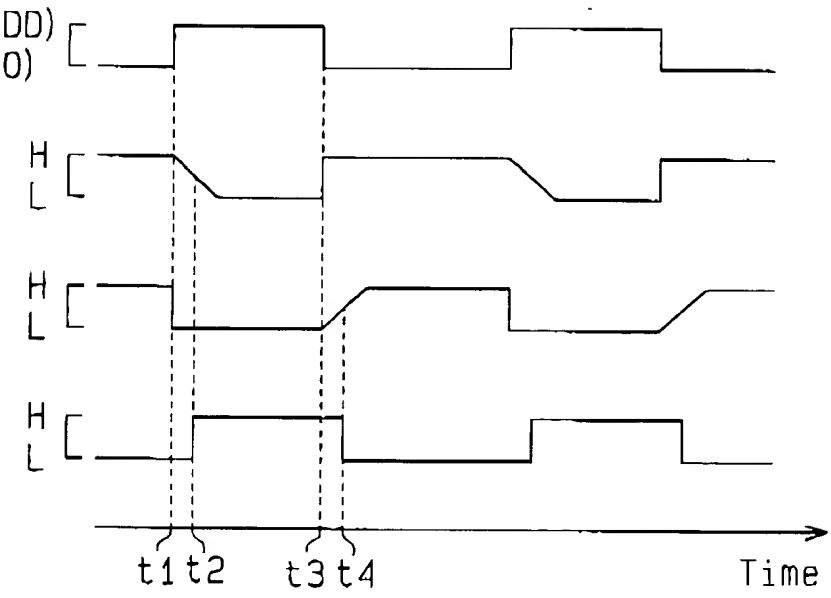


Fig.9

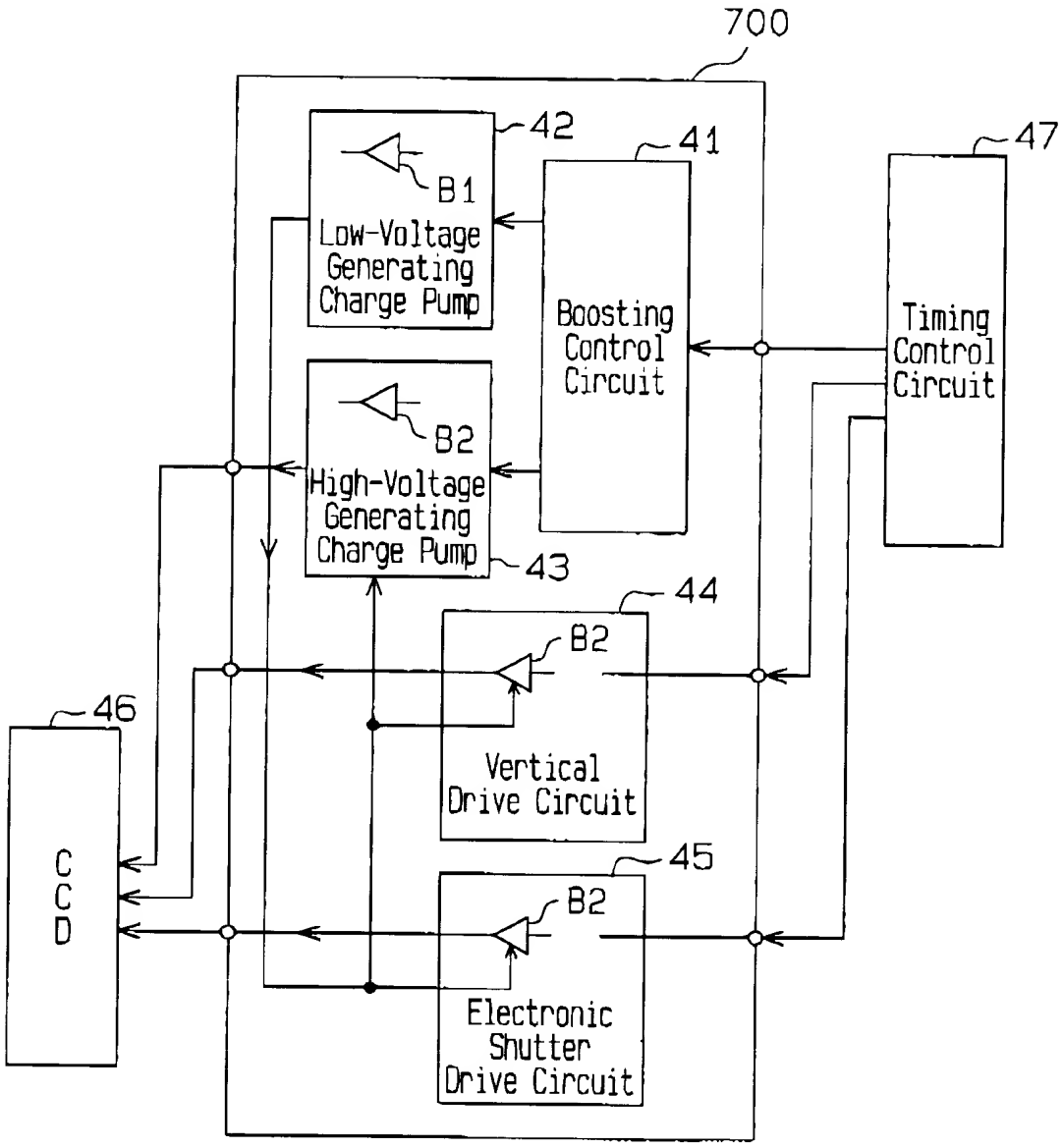
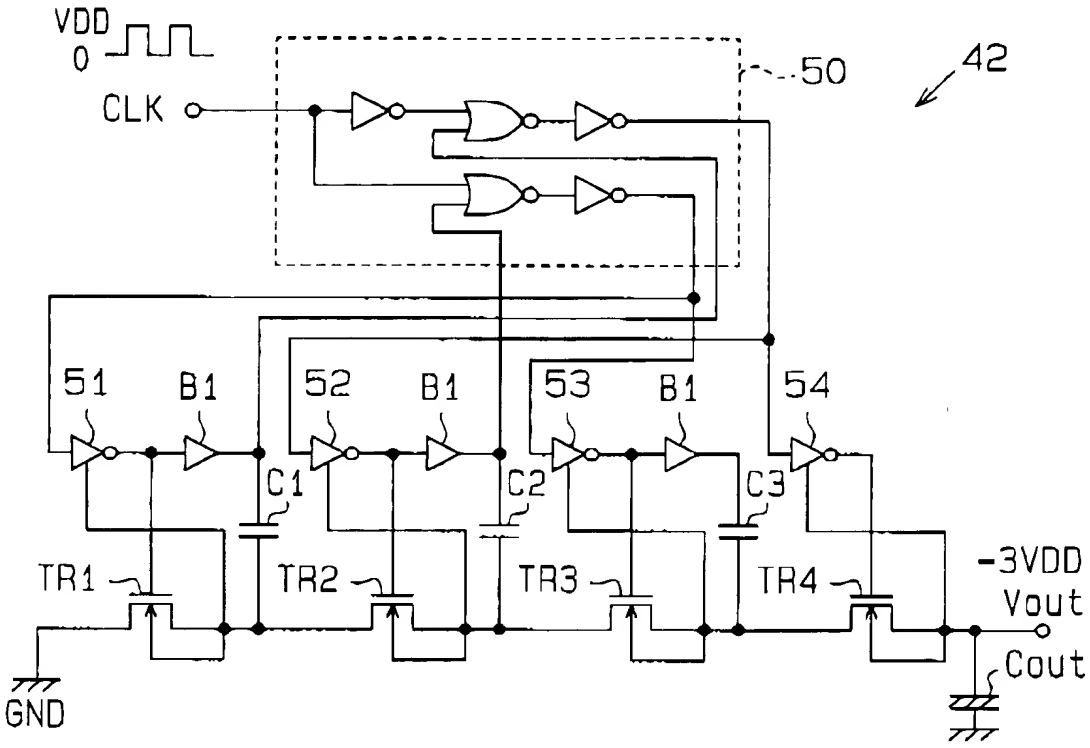

700
42
41
47
B1
Low-Voltage
Generating
Charge Pump
Boosting
Control
Circuit
Timing
Control
Circuit
B2
High-Voltage
Generating
Charge Pump
43
44
B2
Vertical
Drive Circuit
46
C
C
D
45
B2
Electronic
Shutter
Drive Circuit

Fig.10


VDD
0
CLK
50
42
51
B1
52
B1
53
B1
54
C1
C2
C3
TR1
TR2
TR3
TR4
-3VDD
Vout
Cout
GND